DEPARTMENT OF SCIENCE

COURSE OUTLINE – WINTER 2012

CS3290 – COMPUTER ORGANIZATION AND ARCHITECTURE II – 3 (3-0-3) 90 HOURS

INSTRUCTOR: Libero Ficocelli **PHONE:** 780 539 - 2825
OFFICE: C424 **E-MAIL:** LFicocelli@gprc.ab.ca

OFFICE HOURS: TBA

PREREQUISITE(S)/COREQUISITE: CS2290 or Permission of the instructor

REQUIRED TEXT/RESOURCE MATERIALS:

Theory: Digital Electronics – a practical approach with VHDL 9th edition
Willian Kleitz
Pearson Publishing

CALENDAR DESCRIPTION:

This course will introduce students to the fundamentals of logic design and computer architecture. Important topics will include (but not limited to) basic logic gates and circuits, circuit minimization, combinational logic, sequential logic, latches and flip-flops, registers and register transfers, ALU design, Control unit design, CPU design, I/O operations.

CREDIT/CONTACT HOURS: 3 (3-0-3) 90 Hours

DELIVERY MODE(S): In class lecture

OBJECTIVES (OPTIONAL):

TRANSFERABILITY: University of Alberta, University of Calgary, University of Lethbridge, Athabasca University, Augustana Faculty (University of Alberta), King's University College

GRADING CRITERIA:

**** Grade of D or D+ may not be acceptable for transfer to other post-secondary institutions.**

GRANDE PRAIRIE REGIONAL COLLEGE			
GRADING CONVERSION CHART			
Alpha Grade	**4-point Equivalent**	**Percentage Guidelines**	**Designation**
A^{+}	**4.0**	**90 – 100**	**EXCELLENT**
A	**4.0**	**85 – 89**	
A^{-}	**3.7**	**80 – 84**	**FIRST CLASS STANDING**
B^{+}	**3.3**	**77 – 79**	
B	**3.0**	**73 – 76**	**GOOD**
B^{-}	**2.7**	**70 – 72**	
C^{+}	**2.3**	**67 – 69**	**SATISFACTORY**
C	**2.0**	**63 – 66**	
C^{-}	**1.7**	**60 – 62**	
D^{+}	**1.3**	**55 – 59**	**MINIMAL PASS**
D	**1.0**	**50 – 54**	
F	**0.0**	**0 – 49**	**FAIL**
WF	**0.0**	**0**	**FAIL, withdrawal after the deadline**

Students are cautioned that it is their responsibility to contact the receiving institutions to ensure transferability

EVALUATIONS:

Lab/Homework Assignments	30%
Class Quizzes	10%
Midterm	25%
Final Exam	35%

STUDENT RESPONSIBILITIES:

- The Student must pass the theory/concepts portion of the course in order to obtain a passing grade for the term. In other words a student must obtain 50% out of a possible 70 exam based marks - which includes all components except the lab assignments.
- LAB attendance is mandatory. You must clear all absences with me; failure to comply will result in a failing grade for the course!

STATEMENT ON PLAGIARISM AND CHEATING:

Refer to the Student Conduct section of the College Admission Guide at

http://www.gprc.ab.ca/programs/calendar/ or the College Policy on Student Misconduct: Plagiarism and Cheating at www.gprc.ab.ca/about/administration/policies/**

**Note: all Academic and Administrative policies are available on the same page.

COURSE SCHEDULE/TENTATIVE TIMELINE:

- Boolean Algebra (basic identities, algebraic manipulation)
- Logic gates
- Cannonical Forms (minterms, maxterms, SOP, POS)
- Applications of Boolean Algebra
- Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)
- Quine-McCluskey Method
- Multiple Output Networks (analysis and design)
- Decoders/Encoders/Priority Encoders (decoder expansion)
- Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)
- Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)
- Sequential Circuits (Charactersistic/Excitation Tables, state diagrams, analysis and design)
- Mealy/Moore Machines,
- State Minimization
- Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)
- Registers (Shift, Bidirectional shift, Parallel load)
- RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)
- PLDs (ROM, PROM, PLA, PAL)
- VHDL
- Register transfers and Data Paths (registers, buses, ALU, micro-operations, control words)

Other topics including VHDL programming will also be covered