

## DEPARTMENT OF SCIENCE

### COURSE OUTLINE – Winter 2026

#### CS3290 (A3): COMPUTER ORGANIZATION AND ARCHITECTURE II – 3 (3-0-3)

90 Hours over 15 Weeks

Northwestern Polytechnic acknowledges that our campuses are located on Treaty 8 territory, the ancestral and present-day home to many diverse First Nations, Metis, and Inuit people. We are grateful to work, live and learn on the traditional territory of Duncan's First Nation, Horse Lake First Nation and Sturgeon Lake Cree Nation, who are the original caretakers of this land.

We acknowledge the history of this land and we are thankful for the opportunity to walk together in friendship, where we will encourage and promote positive change for present and future generations.

**INSTRUCTOR:** Franco Carlacci

**PHONE:** 780 539 2091

**OFFICE:** C422

**E-MAIL:** fcarlacci@NWPolytech.ca

**OFFICE HOURS:** TBA

#### **CALENDAR DESCRIPTION:**

Digital circuits, combinational systems, memory, register transfer, control logic design, CPU design, and advanced topics on micro-architectures.

**PREREQUISITE(S)/COREQUISITE:** CS2290

#### **REQUIRED TEXT/RESOURCE MATERIALS:**

*I will be providing links to several OER textbooks as well as additional resource material*

Optional Text :

Logic and Computer Design Fundamentals 5<sup>th</sup> edition (older editions acceptable)  
Morris Mano, Charles Kime, Tom Martin  
Pearson Education

**DELIVERY MODE(S):** In class lecture

**COURSE OBJECTIVES:**

Students will be introduced to digital computer architecture and its underlying digital logic including topics such as:

- integrated circuits from basic logic gates to more complex chips (registers and ALUs)
- fundamentals of digital logic analysis and design.
- Boolean Algebra and its relation to circuit design and minimization
- combinational (no memory component) and sequential (memory) logic
- single bit memory to more organized memory such as registers.
- data paths, control unit design and generic CPU design.

**LEARNING OUTCOMES:**

Students will be able to:

- Understand and manipulate Boolean logic
- Design and build combinational circuits to perform a variety of tasks
- Design and build sequential circuits to perform a variety of tasks
- Reduce both sequential and combinational circuits
- Build a simple CPU which will include registers, ALU, data path and all the necessary circuitry required to decode and execute program code presented in a binary format.

**TRANSFERABILITY:**

Please consult the Alberta Transfer Guide for more information. You may check to ensure the transferability of this course at the Alberta Transfer Guide main page

<http://www.transferalberta.ca>.

**\*\* Grade of D or D+ may not be acceptable for transfer to other post-secondary institutions. Students are cautioned that it is their responsibility to contact the receiving institutions to ensure transferability**

**EVALUATIONS:**

Lab/Homework	
Assignments	20%
Class Quizzes	20%
Midterm	25%
Final Exam	35%

## GRADING CRITERIA:

Please note that most universities will not accept your course for transfer credit **IF** your grade is **less than C-**.

Alpha Grade	4-point Equivalent	Percentage Guidelines	Alpha Grade	4-point Equivalent	Percentage Guidelines
A+	4.0	95-100	C+	2.3	67-69
A	4.0	85-94	C	2.0	63-66
A-	3.7	80-84	C-	1.7	60-62
B+	3.3	77-79	D+	1.3	55-59
B	3.0	73-76	D	1.0	50-54
B-	2.7	70-72	F	0.0	00-49

## COURSE SCHEDULE/TENTATIVE TIMELINE:

- Boolean Algebra (basic identities, algebraic manipulation)
- Logic gates
- Canonical Forms (minterms, maxterms, SOP, POS)
- Applications of Boolean Algebra
- Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)
- Quine-McCluskey Method
- Decoders/Encoders/Priority Encoders (decoder expansion)
- Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)
- Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)
- Sequential Circuits (Characteristic/Excitation Tables, state diagrams, analysis and design)
- Mealy/Moore Machines,
- State Minimization
- Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)
- Registers (Shift, Bidirectional shift, Parallel load)
- RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)
- PLDs (ROM, PROM, PLA, PAL)
- VHDL
- Register transfers and Data Paths (registers, buses, ALU, micro-operations,)

## STUDENT RESPONSIBILITIES:

- The Student must pass the theory/concepts portion of the course in order to obtain a passing grade for the term. In other words, a student must obtain 40 out of a possible 80 exam based marks - which includes all components except the lab assignments.
- LAB attendance is **mandatory**. You must clear all absences with me; failure to comply will result in a failing grade for the course!

## STATEMENT ON ACADEMIC MISCONDUCT

Academic Misconduct will not be tolerated. For a more precise definition of academic misconduct and its consequences, refer to the Student Rights and Responsibilities policy available at <https://www.nwpolytech.ca/about/administration/policies/index.html>.

\*\*Note: all Academic and Administrative policies are available on the same page.

## ADDITIONAL INFORMATION:

**Attendance** A student may be debarred from an examination when specific requirements are identified in the Course Outline and when the student's performance does not meet the specified requirements. This usually happens when absences are more than four absences (2 weeks), or if significant assessments like exercises and exam(s) are not completed and submitted for grading before the deadlines published; see Final Examination Policy and Debarred from Examinations; <https://www.nwpolytech.ca/about/administration/policies/fetch.php?ID=37>